Barth Electronics, Inc.
Introduction to VFTLP+
BARTH Model 4012

VFTLP+ was originally developed to provide I-V characteristics of CDM protection and its analysis has been similar to that of TLP data used to analyze HBM protection circuits. VFTLP+ and TLP data are an average of the voltage and current waveforms taken in the measurement window. TLP for HBM circuit analysis provides very reasonable average voltage and current data after their waveforms have settled down and are relatively constant.

HBM failures are primarily the result of energy dissipation in silicon protection elements. CDM threats are 1 to 2 ns long, while HBM treats are about 100 to 200 ns long. CDM is different from HBM in two important respects. First, CDM currents create voltages which are applied to gate oxides. Oxides fail when their voltage capability is exceeded.

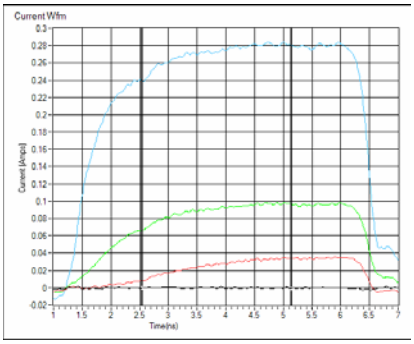
The second major difference is that HBM testing specifies 2 to 10 ns current risetimes while the CDM event is extremely fast. Its risetime is as fast as 100 ps and the length of its pulses are much shorter. In order for VFTLP+ to simulate CDM events its test pulse risetimes must be as fast as this 100 ps. The original VFTLP+ test system used shorter pulses with the intention of simulating CDM. However this test still uses the IV data averaged in the measurement window. Although averaged data is useful in understanding the basic I-V characteristics of the CDM protection element, it misses time varying information. The high speed CDM event creates rapidly changing current and voltages in the silicon protection elements or circuits. Understanding their high speed response introduces a new and very important indicator of CDM protection circuit operation, that is impossible to identify using only current and voltage data averaged during a measurement window.

Because the primary cause of failure with CDM is gate oxide failure, voltage is the primary information needed to understand protection elements or circuits. The high speed CDM event creates very fast rates of current and voltage rise inside high speed IC's. We have developed special 30 ps risetime voltage and current sensors to identify the total DUT response with our VFTLP system. Measuring the high speed operation of silicon elements or circuits on wafer provides a new insight into previously un-known details of protection element operation.

Our VFTLP+ also adds true 100 ps risetime test pulse capability to simulate the CDM testing and CDM events. To deliver the high speed test pulse to the DUT, we always use very low loss transmission lines. Our very high speed wafer probes achieve extremely low inductance connections to the wafer. We identify this carefully engineered CDM circuit analysis tool as VFTLP**+**.

Our measurements of protection circuits on wafer have identified oxide threat Time Dependent Dielectric Breakdown (TDDB) voltages. Until now this measurement has been made with rectangular pulses to identify oxide voltage sensitivities to relatively short pulses. We have found that the first part of the oxide voltage threat is the initial voltage impulse. We identify this as the Initial Voltage Impulse (IVI) because it occurs in every VFTLP**+** and CDM event. It is caused when extremely fast CDM events

create very narrow voltage impulses, typically being 150 to 200 picoseconds wide. More complex protection circuits take additional time to turn-on and the IVI fall time can be as long as 5 ns. The IVI precedes the average steady state voltage identified in the measurement window. The IVI voltage has been referred to in previous papers although the true peak voltage has not been available. With both limited risetime test pulses and limited DUT response risetime measurement systems, the real silicon IVI cannot be determined. The total oxide threat can now be identified by measurements of the voltage created by silicon protection circuits during the total time the threat is applied.



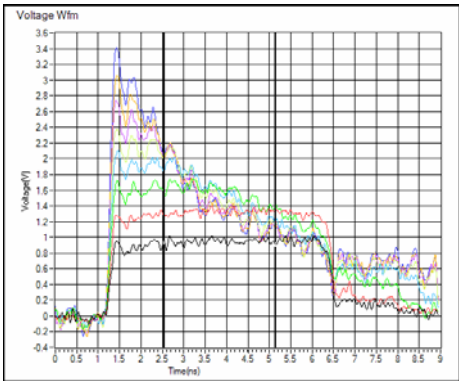
Current wave forms of 1N4448 diode from 0 to 0.27 amps

The ability to simulate CDM rates of rise and measure its effect on silicon protection circuits is provided in the VFTLP**+** test. It demonstrates the high speed measurement capabilities needed to understand the high speed operation of silicon. Commercial diodes do not fail at the highest pulse current and longest pulses. They are readily available and their time delay characteristics are very repeatable.

The waveform and I-VV plot data provided by this VFTLP**+** test adds completely new analysis to the original VFTLP+ system. Improving CDM protection is important because the sensitivity of gate oxides continues to increase.

This new analysis tool can provide an important data base for ESD design. This information will be the first time manufacturers of wafers will be able to see the complete protection element characteristics at the high speeds which simulate the CDM test.

The wafer information we measure and publish will be isolated from other manufacturers.



Voltage waveforms measured over 0 to 1 amp range. For clarity, only every third waveform is shown.

We will continue to develop a better understanding of circuit response to high speed threats. This test method can begin a correlation between voltage response and variations in geometry. Voltage and current waveforms on future silicon CDM protection will become more analytical as dimensional details are better understood. We can provide this information to begin a better understanding of previously hidden operational parameters of high speed ESD protection.

This first presentation demonstrates how ordinary VFTLP+ has been improved to expand design data it is now possible to extract from CDM protection elements. We have devoted over two years to this test system and will continue to expand the value of this new analysis tool.

Our measurements of actual CDM protection circuits and individual test structures data will continue. This new source of data begins a new ability to analyze the high speed operation of silicon elements and circuits in continuous time detail.

Adapted from Barth 4012 Application Note #2.

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